

What is claimed is:

- Sub A1
1. A cache directory configuration method for maintaining coherence between a plurality of caches, wherein each cache comprises a copy of a section of said main memory, said method comprising:
    - storing copies of address tags stored in said plurality of caches in a cache directory, wherein said cache directory is divided into a plurality of parts; and
    - processing a plurality of search requests concurrently using said plurality of parts.
  2. The cache directory configuration method of claim 1 further comprising:
    - partitioning a search address tag associated with said search request into a plurality of sections;
    - responsive to said search request, determining if a first section of said plurality of sections matches an entry in a first part of said plurality of parts; and
    - when no match is indicated for any entry in said first part, returning a result.
  3. The cache directory configuration method of claim 2, further comprising:
    - when a match is indicated for any entry in said first part, determining if a second section of said plurality of sections matches an entry in a second part of said plurality of parts.
  4. The cache directory configuration method of claim 1 wherein:
    - each entry in said cache directory is divided up into a plurality of entry groups; and
    - each entry group can be operated on independently.
  5. The cache directory configuration method of claim 1 wherein the plurality of parts comprises a first sub directory having even bits of each entry in the

3 cache directory and a second sub directory having odd bits of each entry in the cache  
4 directory.

1 6. The cache directory configuration method of claim 1 further  
2 comprising:  
3 responsive to a search request of said plurality of search requests,  
4 determining if said search request matches any entry in a part of said plurality of parts;  
5 and  
6 when a match is indicated, returning a result.

1 7. An information processing device comprising:  
2 a plurality of processing devices, each of said plurality of processing  
3 devices comprising a cache storage module storing a copy of a section of a main storage  
4 device;  
5 the main storage device shared by said plurality of processing devices and  
6 formed as a plurality of banks, wherein said banks having different address spaces and  
7 capable of operating in parallel; and  
8 a coherence control device comprising a cache directory for providing coherence between  
9 a cache storage module and said main storage device, said cache directory storing copies  
10 of address tags associated with said cache storage module, said cache directory being  
11 divided into a plurality of units capable of operating in parallel, and said coherence  
12 control device processing a plurality of search requests concurrently using said plurality  
13 of units

1 8. A method for searching a cache directory comprising a plurality of  
2 address tags, said address tags copied from a cache of a plurality of caches in a system  
3 with a plurality of processors, said plurality of processors sharing a main memory,  
4 wherein each cache is associated with a processor, said method comprising:  
5 receiving a search request address tag;  
6 partitioning said search request address tag into a first plurality of sections;  
7 partitioning each address tag of said plurality of address tags into a second  
8 plurality of sections;  
9 comparing for each address tag, a first section of said first plurality of  
10 sections with a first section of said second plurality of sections; and

11           returning a result when said comparing indicates no match for any address  
12 tag of said plurality of address tags.

1           9.       The method of claim 7, wherein when said comparing indicates a  
2 match for any address tag of said plurality of address tags, further comparing for each  
3 address tag, a second section of said first plurality of sections with a second section of  
4 said second plurality of sections.

1           10.     A method for searching a cache directory used to maintain  
2 coherence between a cache and a main memory, comprising a plurality of memory banks,  
3 in a multi-processor system, the cache directory, comprising a plurality of sections, the  
4 method comprising:

5                 receiving a write request address by the cache directory to the main  
6 memory from another processor;

7                 determining from the write request address a memory bank of the plurality  
8 of memory banks;

9                 selecting a section of the plurality of sections associated with the memory  
10 bank; and

11                 searching the section for the write request address.

1           11.     The method of claim 10 wherein the determining includes using a  
2 bit of the write request address.

1           12.     The method of claim 10 wherein the section comprises every other  
2 entry in the cache directory.

1           13.     A system for searching a cache directory used to maintain  
2 coherence between a cache and a main memory, comprising a plurality of memory banks,  
3 in a multi-processor system, the cache directory, comprising a plurality of sub-directories,  
4 each subdirectory associated with a memory bank of the plurality of memory banks, the  
5 system comprising:

6                 an input module for receiving a plurality of requests to the cache directory;

a crossbar switch for coupling the input module with the plurality of sub-directories; and

a control module for routing a first request of the plurality of requests to a first subdirectory of the plurality of sub-directories and a second request of the plurality of requests to a second subdirectory of the plurality of sub-directories for concurrent searching of the first and second subdirectories, when the first and second requests address different memory banks of the plurality of memory banks.

14. A method for searching a cache directory used in maintaining coherence among caches in a multiprocessor system, comprising:  
 partitioning the cache directory into a plurality of parts, wherein each part of the plurality of parts is searched concurrently with another part of the plurality of parts;  
 partitioning a plurality of requests to the cache directory into a plurality of sub-requests, wherein each sub-request corresponds to a part of the plurality of parts; and  
 searching in parallel, each part using an associated sub-request.

15. The method of claim 14 wherein each part is associated with a memory bank of the multiprocessor system

16. The method of claim 14 wherein a sub-request of the plurality of sub-requests comprises the even bits of the request.

17. The method of claim 14 wherein a part of the plurality of parts has entries which are an odd entries in the cache directory.

18. A cache directory configuration system for maintaining coherence between a plurality of caches, wherein each cache comprises a copy of a section of said main memory, said system comprising:

a cache directory, comprising copies of address tags stored in said plurality of caches, wherein said cache directory is divided into a plurality of parts; and  
 a plurality of units for processing a plurality of search requests concurrently using said plurality of parts.

1 19. The cache directory configuration system of claim 18 further  
2 comprising:  
3 a selector module for partitioning a search address tag associated with said  
4 search request into a plurality of sections; and  
5 a first comparison module, responsive to said search request, for  
6 determining if a first section of said plurality of sections matches an entry in a first part of  
7 said plurality of parts and when no match is indicated for any entry in said first part,  
8 returning a result.

1 20. The cache directory configuration system of claim 19, further  
2 comprising:  
3 when a match is indicated for any entry in said first part, a second  
4 comparison module for determining if a second section of said plurality of sections  
5 matches an entry in a second part of said plurality of parts.

1 21. The cache directory configuration system of claim 18 wherein:  
2 each entry in said cache directory is divided up into a plurality of entry  
3 groups; and  
4 each entry group can be operated on independently.

1 22. The cache directory configuration system of claim 18 wherein the  
2 plurality of parts comprises a first sub directory having even bits of each entry in the  
3 cache directory and a second sub directory having odd bits of each entry in the cache  
4 directory.

1 23. The cache directory configuration system of claim 18 further  
2 comprising:  
3 a comparison module, responsive to a search request of said plurality of  
4 search requests, for determining if said search request matches any entry in a part of said  
5 plurality of parts, and when a match is indicated, returning a result.

1 24. A system for searching a cache directory used to maintain  
2 coherence between a cache and a main memory, comprising a plurality of memory banks,  
3 in a multi-processor system, the cache directory, comprising a plurality of sections, the  
4 system comprising:

5 an input module for receiving a write request address by the cache  
6 directory from another processor;  
7 a bank selector module for determining from the write request address, a  
8 memory bank of the plurality of memory banks;  
9 a switch for selecting a section of the plurality of sections associated with  
10 the memory bank; and  
11 a comparison module for searching the section for the write request  
12 address.  
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